



Welcome United States Patent and Trademark Office

☐ Search Results

BROWSE

SEARCH

IEEE XPLORE GUIDE

Results for "((((bios or post)<near/30> test\* <near/30> configurat\* <near/50> (chip\* or circuit..." ☒ e-mail

Your search matched 5 of 1372086 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by **Relevance** in **Descending** order.

## » Search Options

[View Session History](#)[New Search](#)

## Modify Search

 
☐ Check to search only within this results set
Display Format: ☒ Citation ☐ Citation & Abstract

## » Key

IEEE JNL IEEE Journal or Magazine

IEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

 [Select All](#) [Deselect All](#)

- ☐ **1. Transistor-limited constant voltage stress of gate dielectrics**  
 Linder, B.P.; Frank, D.J.; Stathis, J.H.; Cohen, S.A.;  
[VLSI Technology, 2001. Digest of Technical Papers. 2001 Symposium on 12-14 June 2001 Page\(s\):93 - 94](#)  
 Digital Object Identifier 10.1109/VLSIT.2001.934965  
[AbstractPlus](#) | Full Text: [PDF\(168 KB\)](#) IEEE CNF  
[Rights and Permissions](#)
- ☐ **2. Testing programmable interconnect systems: an algorithmic approach**  
 Liu, B.; Lombardi, F.; Huang, W.K.;  
[Test Symposium, 2000. \(ATS 2000\). Proceedings of the Ninth Asian 4-6 Dec. 2000 Page\(s\):311 - 316](#)  
 Digital Object Identifier 10.1109/ATS.2000.893642  
[AbstractPlus](#) | Full Text: [PDF\(504 KB\)](#) IEEE CNF  
[Rights and Permissions](#)
- ☐ **3. Post-arc current measurement down to the ten milliamperes range**  
 Barrault, M.; Bernard, G.; Maftoul, J.; Rowe, S.;  
[Power Delivery, IEEE Transactions on Volume 8, Issue 4, Oct. 1993 Page\(s\):1782 - 1788](#)  
 Digital Object Identifier 10.1109/61.248285  
[AbstractPlus](#) | Full Text: [PDF\(408 KB\)](#) IEEE JNL  
[Rights and Permissions](#)
- ☐ **4. Design and implementation of a parity-based BIST scheme for FPGA glot**  
 Xiaoling Sun; Xu, S.; Jian Xu; Trouborst, P.;  
[Electrical and Computer Engineering, 2001. Canadian Conference on Volume 2, 13-16 May 2001 Page\(s\):1251 - 1257 vol.2](#)  
 Digital Object Identifier 10.1109/CCECE.2001.933621  
[AbstractPlus](#) | Full Text: [PDF\(596 KB\)](#) IEEE CNF  
[Rights and Permissions](#)
- ☐ **5. A structural test methodology for SRAM-based FPGAs**  
 Renovell, M.;  
[Integrated Circuits and Systems Design, 2002. Proceedings. 15th Symposium 9-14 Sept. 2002 Page\(s\):385](#)  
 Digital Object Identifier 10.1109/SBCCI.2002.1137687

[AbstractPlus](#) | Full Text: [PDF\(182 KB\)](#) [IEEE CNF](#)  
[Rights and Permissions](#)

Indexed by  
 Inspec®

[Help](#) [Contact Us](#) [Privacy & :](#)

© Copyright 2006 IEEE –